Claim 3 (allowed) The device in claim 1 wherein the doped region within the semiconductor substrate is electrically in series with an electrical load other than itself.

Claim 4 (allowed) The device in claim 1 wherein the doped region within the semiconductor substrate is utilized as a resistive load for an electronic component or power supply circuit.

Claim 5 (original) A heat dissipating IC device comprising:

at least one IC die comprising a semiconductor substrate including at least one circuitry layer with a hot region on at least one substrate face;

at least one electrically conductive or semiconductive member attachable to the semiconductor substrate; and

an electrical source connected to the electrically conductive or semiconductive member, whereby the charge carrier flow travels in a direction from the hotter region on the semiconductor substrate face outward toward the perimeter of the substrate face.

Claim 6 (original) The device in claim 5 wherein an electric via connects a portion of the circuitry layer with the semiconductor substrate in order to provide electrical power to the electrically conductive member.

Claim 7 (original) The device in claim 5 wherein the electrically conductive member is electrically in series with an electrical load other than itself.

Claim 8 (canceled)

Claim 9 (canceled)

Claim 10 (original) The device in claim 5 wherein the semiconductor substrate is attached to the electrically conductive or semiconductive member by wafer bonding.

Claim 11 (original) The device in claim 5 wherein the electrically conductive or semiconductive member is attached to more than one semiconductor substrate.

Claim 12 (original) The device in claim 5 wherein the semiconductor substrate attachment to the conductive or semiconductive member is electrically conductive.

Claim 13 (allowed) A heat dissipating IC device comprising:

at least one IC die comprising a semiconductor substrate including at least one circuitry layer on at least one substrate face;

at least one thermoelement couple, said couple comprised of the semiconductor substrate and at least one dissimilar conductor electrically bonded to the semiconductor substrate thereby creating junctions; and

said thermoelement couple comprises at least one heat absorbing junction and at least one heat rejecting junction wherein the heat absorbing junction is positioned near the center of the substrate face and the heat rejecting junction is positioned near the perimeter of the substrate face.

Claim 14 (allowed) The device in claim 13 wherein the semiconductor substrate, adjacent the junctions, includes a doped region thereby creating a depletion layer between the substrate and doped region.

Claim 15 (allowed) The device in claim 13 wherein the dissimilar conductor comprises more than one layer.

Claim 16 (allowed) The device in claim 13 wherein an electric via connects a portion of the circuitry layer with

the semiconductor substrate in order to provide electrical power to the thermoelement couple junctions.

Claim 17 (allowed) The device in claim 13 wherein a voltage is applied to the thermoelement couple.

Claim 18 (allowed) The device in claim 13 wherein the thermoelement couple is electrically in series with an electrical load other than itself.

Claim 19 (allowed) The device in claim 13 wherein the thermoelement couple is utilized as a resistor for an electronic component.

Claim 20 (allowed) The device in claim 13 wherein a voltage and current is generated by the thermoelement couple and is consumed by an external electric load.

Claim 21 (allowed) The device in claim 13 wherein the silicon substrate and dissimilar thermoelement, comprising each thermoelement couple, is electrically bonded to each other at both the heat absorbing and heat rejecting junctions thereby creating closed electrical circuit thermoelement couples.

Claim 22 (amended) A heat dissipating IC device including at least one IC die comprising a semiconductor substrate including at least one circuitry layer, the substrate attachable to a heat sink/spreader structure comprising:

a heat sink/spreader structure wherein at least one thermoelement couple is created through the bonding between at least one semiconductor to at least one dissimilar conductor; and

the dissimilar conductor comprises at least one heat absorbing junction and one heat rejecting junction wherein the heat absorbing junction is positioned near the center of the

device and the heat rejecting junction is positioned near the perimeter of the device.

Claim 23 (canceled)

Claim 24 (original) The device in claim 22 wherein the dissimilar conductor and semiconductor each comprise more than one layer.

Claim 25 (canceled)

Claim 26 (original) The device in claim 22 wherein the semiconductor substrate is attached to the heat sink/spreader structure by wafer bonding.

Claim 27 (canceled)

Claim 28 (original) The device in claim 22 wherein the heat rejecting junctions are located outside the bond line between the semiconductor substrate and heat sink/spreader structure.

Claim 29 (original) The device in claim 22 wherein the heat sink/spreader structure is attached to more than one semiconductor substrate.

Claim 30 (canceled)

Claim 31 (original) The device in claim 22 wherein the thermoelement couple is electrically in series with an electrical load other than itself.

Claim 32 (canceled)

Claim 33 (canceled)

Claim 34 (original) The device in claim 22 wherein the semiconductor substrate attachment to the heat sink/spreader structure is electrically conductive.

Claim 35 (allowed) A method of manufacturing a heat dissipating IC device including at least one IC die comprising a semiconductor substrate including at least one circuitry layer on at least one substrate face, more than one thermoelement couple, each with at least one heat absorbing and one heat rejecting junction and P-type and N-type conductive dopants comprising:

(a) Selectively depositing the P and N-type dopants into at least one face of the substrate to form a pattern of P and N-type conductive thermoelements within the semiconductor substrate;

(b) Electrically bonding the P and N-type conductivity thermoelements at heat absorbing and heat rejecting junctions to form thermoelement couples.

Claim 36 (allowed) The method of claim 35 wherein the heat absorbing junctions are positioned near the center of the semiconductor substrate face and the heat rejecting junctions are positioned near the perimeter of the substrate face.

Claim 37 (allowed) The method of claim 35 wherein a dielectric, such as oxide or nitride, is added to the physical regions between each P and N-type thermoelement in order to provide electrical insulation between each thermoelement.

Claim 38 (allowed) The method of claim 35 wherein the physical regions between each P and N-type thermoelement are removed in order to provide electrical insulation between each thermoelement.

Claim 39 (allowed) The method of claim 35 wherein a voltage is applied to at least one thermoelement couple.

Claim 40 (allowed) The method of claim 35 wherein at least one thermoelement couple is electrically in series with an electrical load other than itself.

Claim 41 (allowed) The method of claim 35 wherein at least thermoelement couple is utilized as a resistive load for an electronic component.

Claim 42 (allowed) The method of claim 35 wherein a voltage and current is generated by at least one thermoelement couple and is consumed by an external electric load.

Claim 43 (amended) A heat dissipating IC device including at least one IC die comprising at least one semiconductor substrate including at least one circuitry layer on at least one substrate face, more than one thermoelement couple stage, each stage containing at least one thermoelement couple, each with at least one heat absorbing and heat rejecting junction, wherein <u>each heat absorbing junction is positioned near the center of each thermoelement couple stage and heat rejecting junction is positioned near the perimeter of each stage</u> and all thermoelement couple stages are fabricated within at least one semiconductor substrate.

Claim 44 (original) The device in claim 43 wherein each successive thermoelement couple stage is laterally displaced from the previous stage and the heat source or object to be cooled.

Claim 45 (original) The device in claim 43 wherein each stage is positioned outside the entire perimeter of the previous stage and each successive stage.

Claim 46 (canceled)